

Computer Architecture -22966-

- Carlos J. Barrios H., PhD.
- cbarrios@uis.edu.co
- @carlosjaimebh



"Sure, it will be an eyesore, but after we build a lot of them, it'll fit right in!"

Business vs Engineering

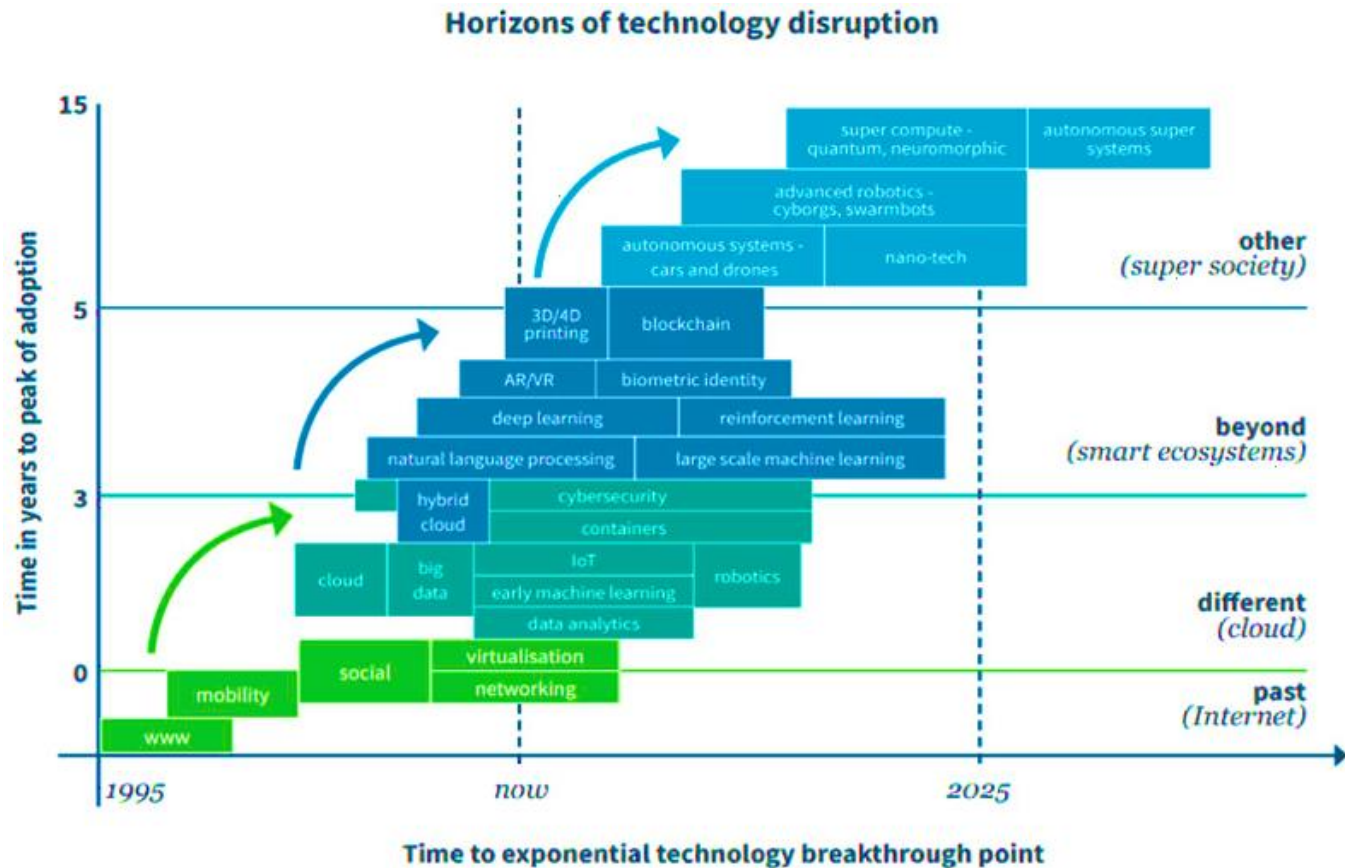
The screenshot shows the Intel Processor Diagnostic Tool interface. The 'System Information' section on the left lists system details such as the processor name (Intel(R) Core(TM) i5-4670 CPU @ 3.40GHz), memory (8 GB), and operating system (Microsoft Windows 10 Pro 64-bit). The 'Test Status' section shows a red bar indicating a 'FAIL' result for Processor 1. A large red box with the word 'FAIL' in white is prominently displayed. Below this, a log shows the test result: 'IPDT64 - Result: Fail'. The 'Test' section on the right contains a table of test modules and their statuses.

Test Module	Status	Test	Status
Genuine Intel	Pass	MMXSSE	<input checked="" type="checkbox"/>
Temperature	Pass	AVX	<input checked="" type="checkbox"/>
Brand String	Pass	IMC	<input checked="" type="checkbox"/>
CPU Frequency	Fail	PCH	<input checked="" type="checkbox"/>
Floating Point	<input checked="" type="checkbox"/>	IGD	<input checked="" type="checkbox"/>
Prime Num Gen	<input checked="" type="checkbox"/>	GFX	<input checked="" type="checkbox"/>
Cache	<input checked="" type="checkbox"/>	CPU Load	<input checked="" type="checkbox"/>
* Click Status result after test completes for more info		Stop Testing On Fail	<input checked="" type="checkbox"/>

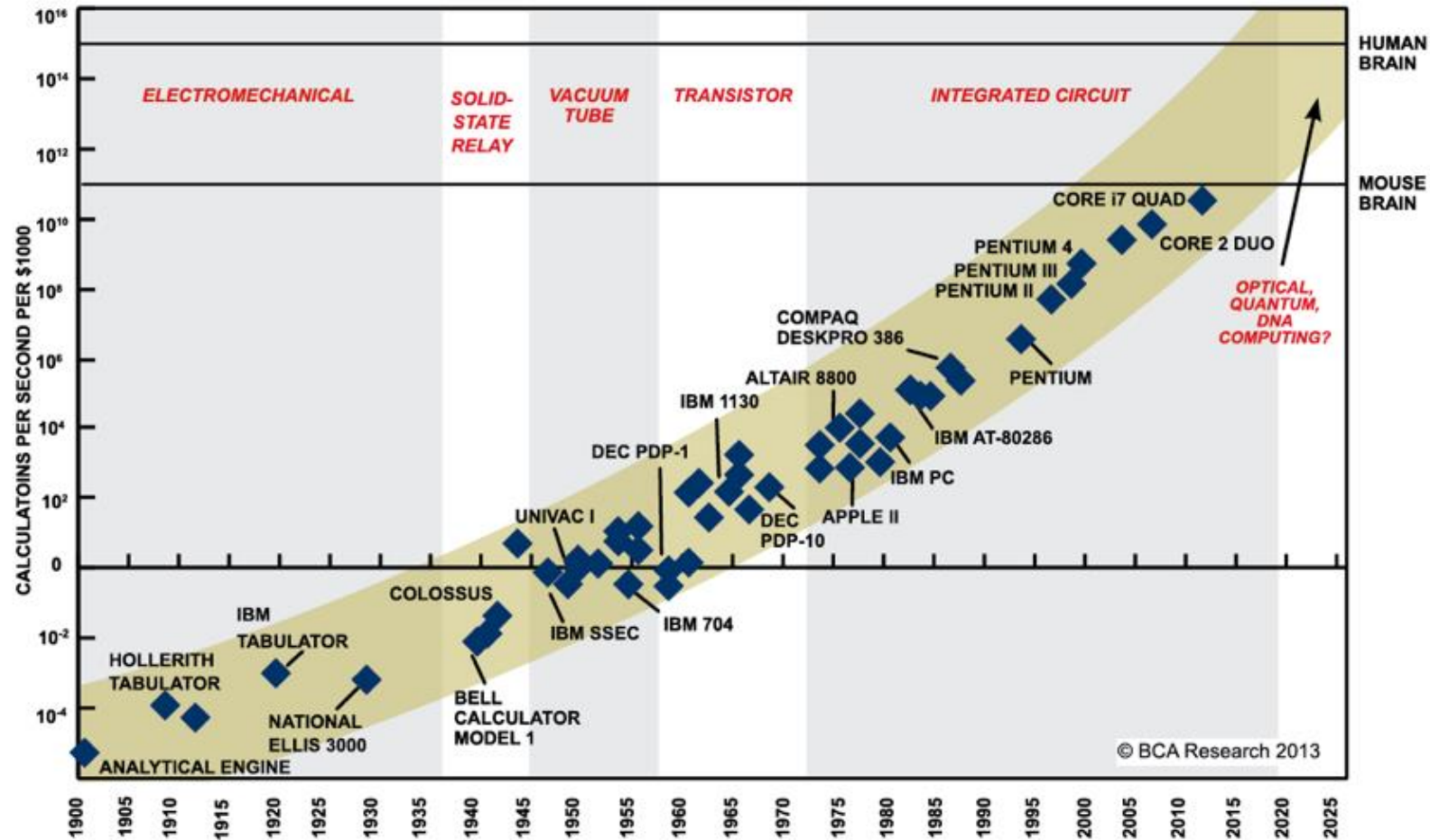
« The problem seems to be that elevated operating voltages have led to instability and even processor failures, requiring a microcode update ».

https://www.theregister.com/2024/08/09/opinion_column_intel/

New Computing – New Humans



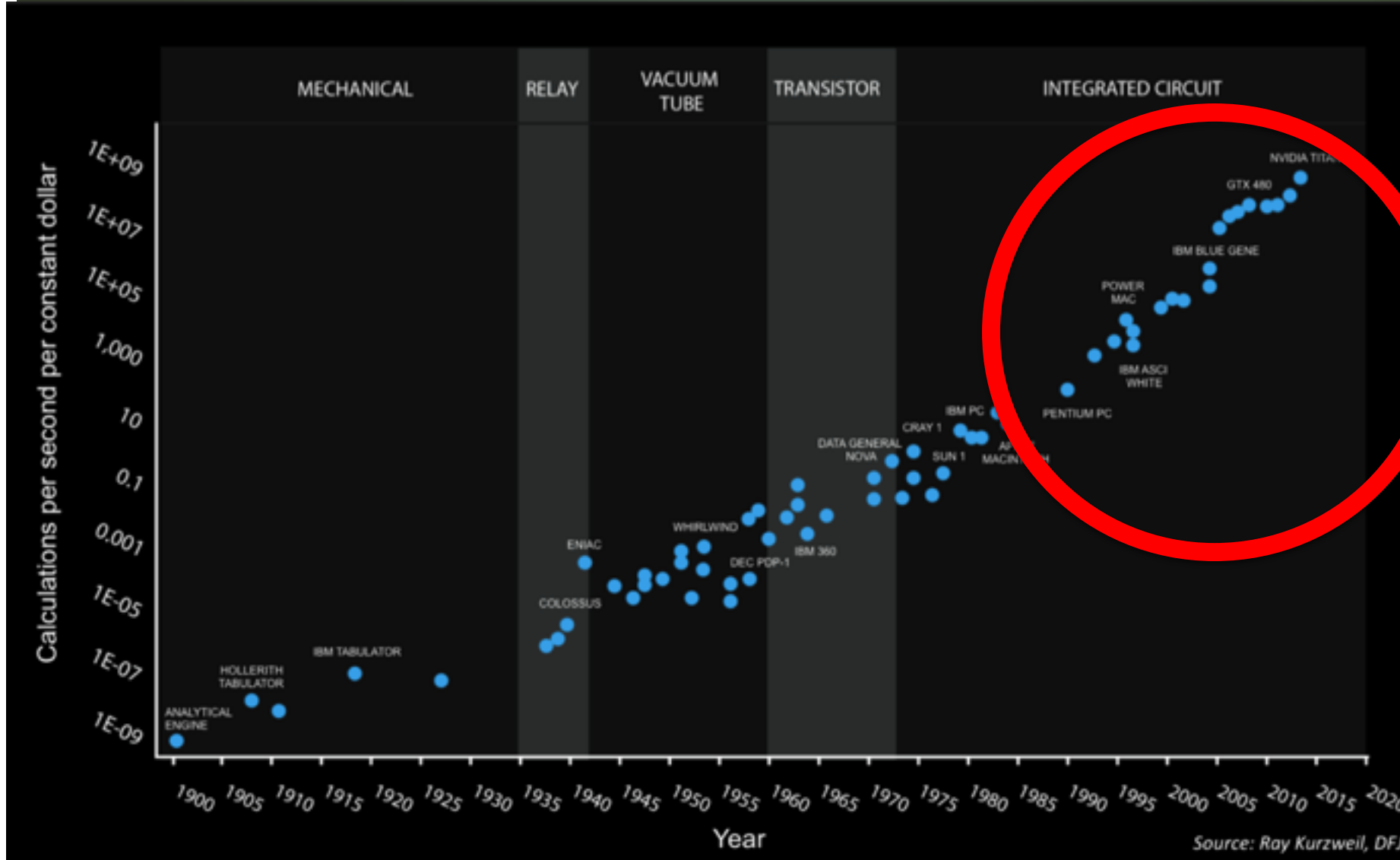
Computer Disruption



SOURCE: RAY KURZWEIL, "THE SINGULARITY IS NEAR: WHEN HUMANS TRANSCEND BIOLOGY", P.67, THE VIKING PRESS, 2006. DATAPPOINTS BETWEEN 2000 AND 2012 REPRESENT BCA ESTIMATES.

The (Post) Moore Era

6

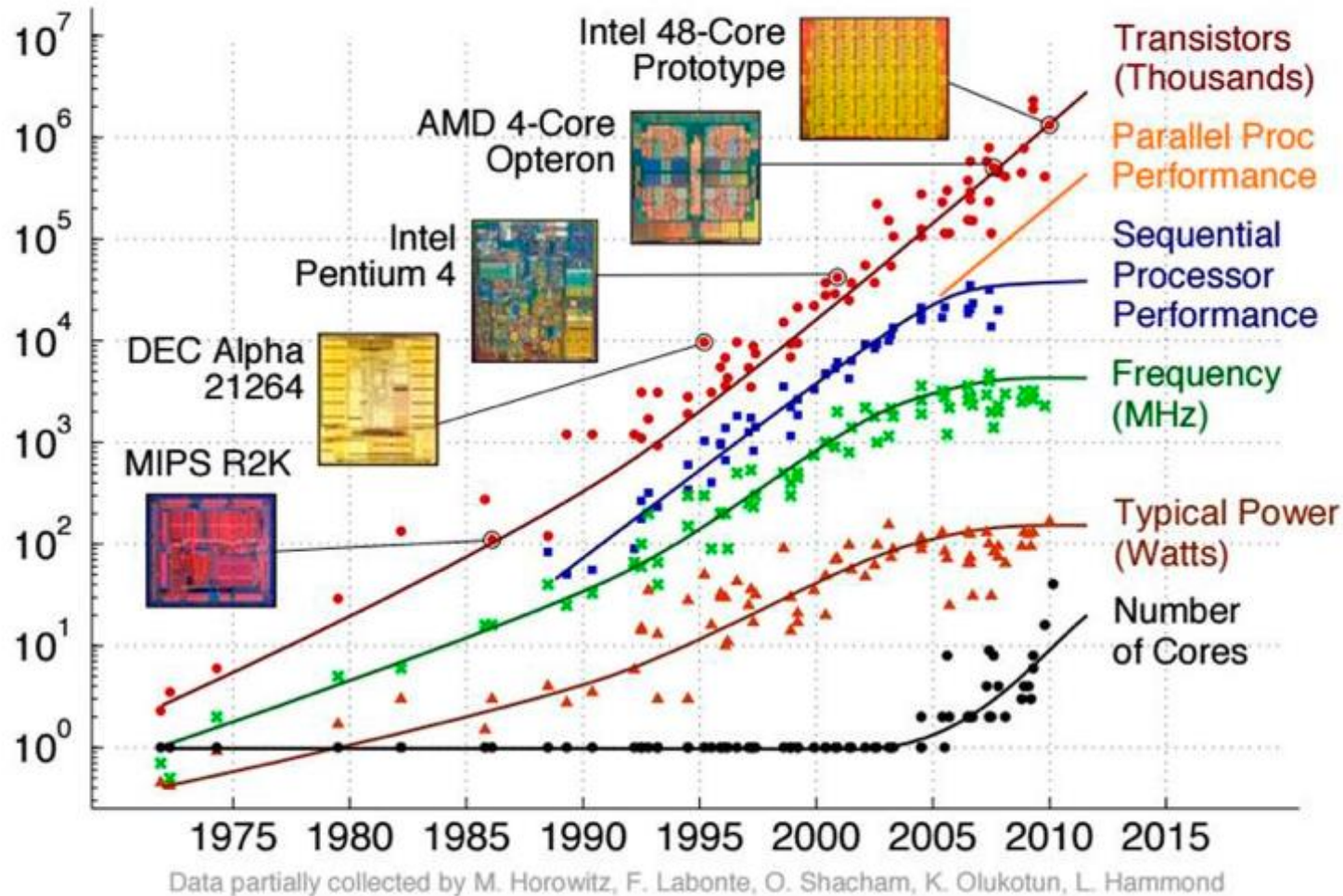


After 120 years... The Moore's Law is Dead



Jack Dongarra

Computer (Moore?) Disruption



Gordon Moore
1929 - 2023



Gordon Moore pass away March 24/2023

The Cambrian Explosion in Architecture for AI

8

Satoshi Matsouka Vision



CPU



RAM



GPU

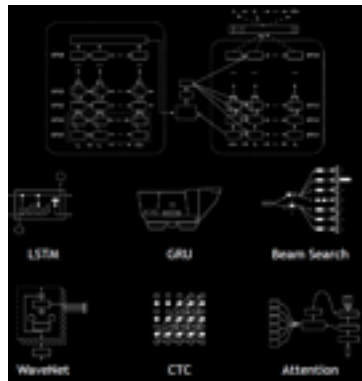


Storage

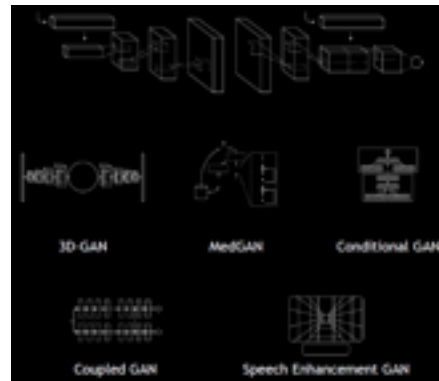
Convolution Networks



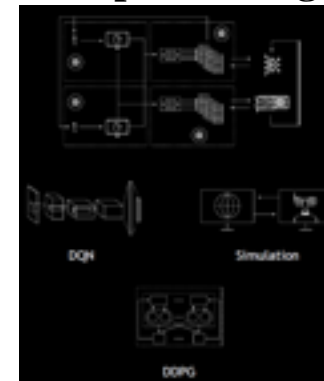
Recurrent Networks



AR Networks



Deep Learning



New Networks



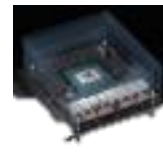
RPI



Nano



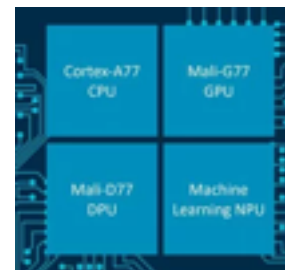
TX2



Xavier



FPGA



SiP



ASIC

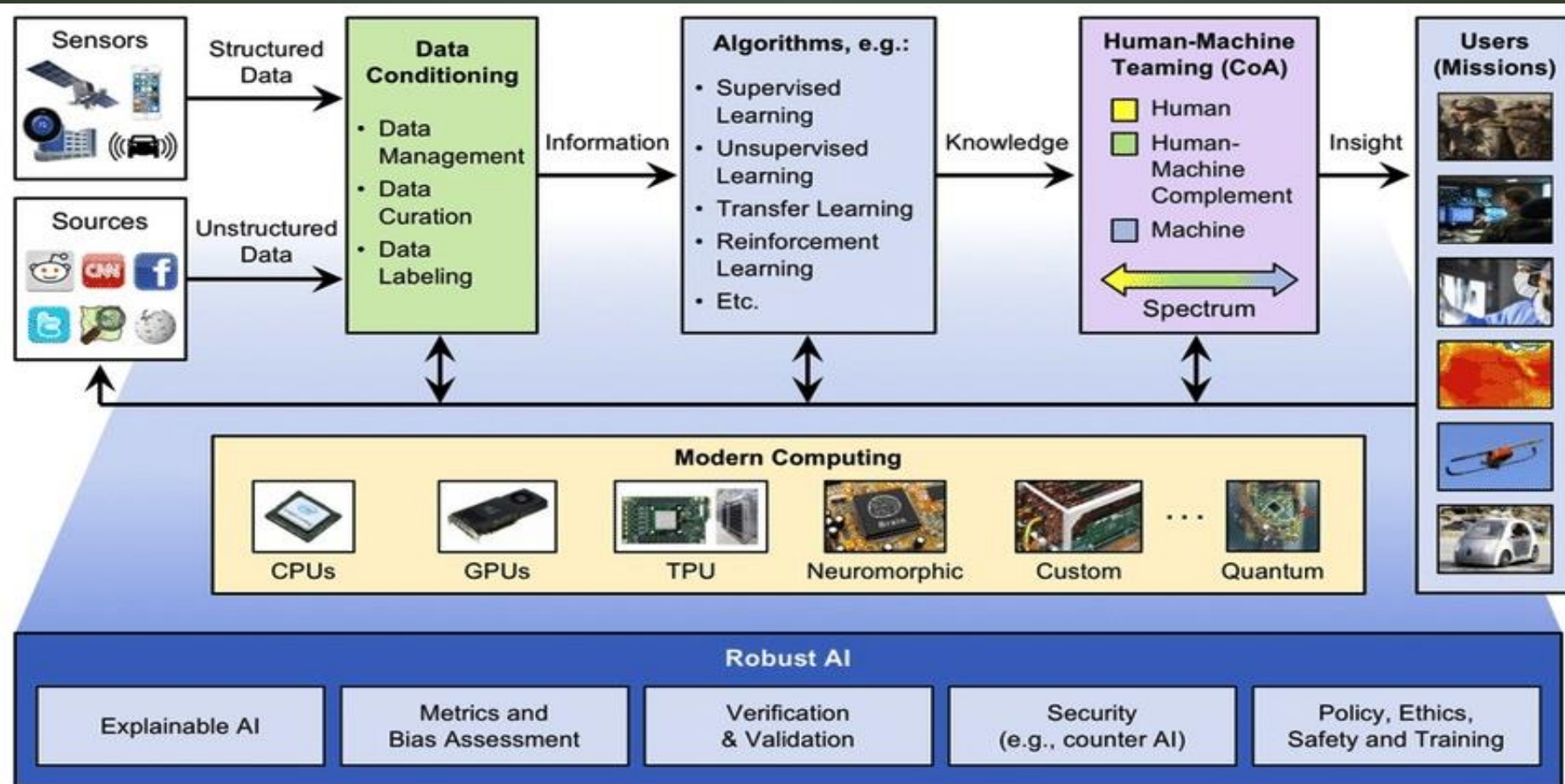


TPU



V100

Canonical Architecture for AI



CoA = Courses of Action

GPU = Graph Processing Unit

TPU = Tensor Processing Unit

Computer Architecture Representation (1/2)

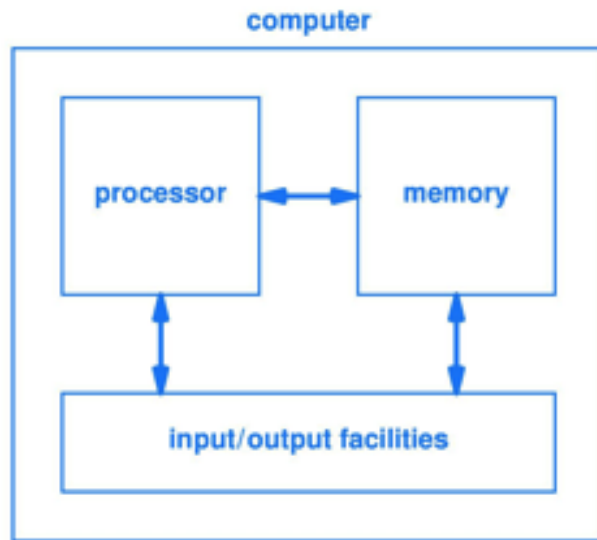


Illustration of the Von Neumann Architecture. Both programs and data can be stored in the same memory.

From <https://eca.cs.purdue.edu/index.html>

- ▶ Von Neumann Representation
 - ▶ Von Neumann Computer Machines
 - ▶ Classical Computers
- ▶ Input
- ▶ Processor
- ▶ Memory
- ▶ Output

Computer Architecture Representation (2/2)

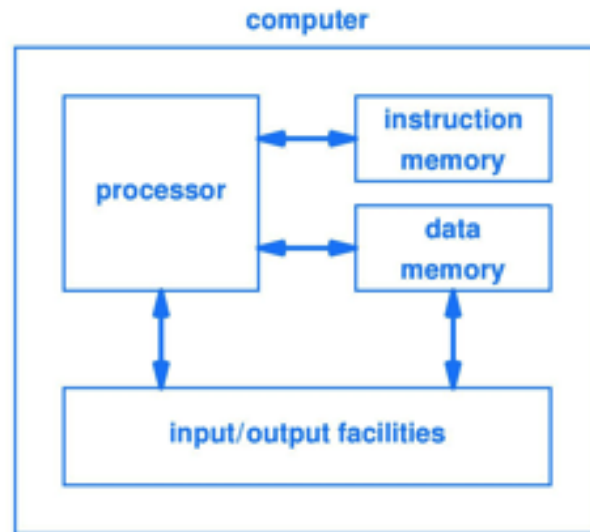
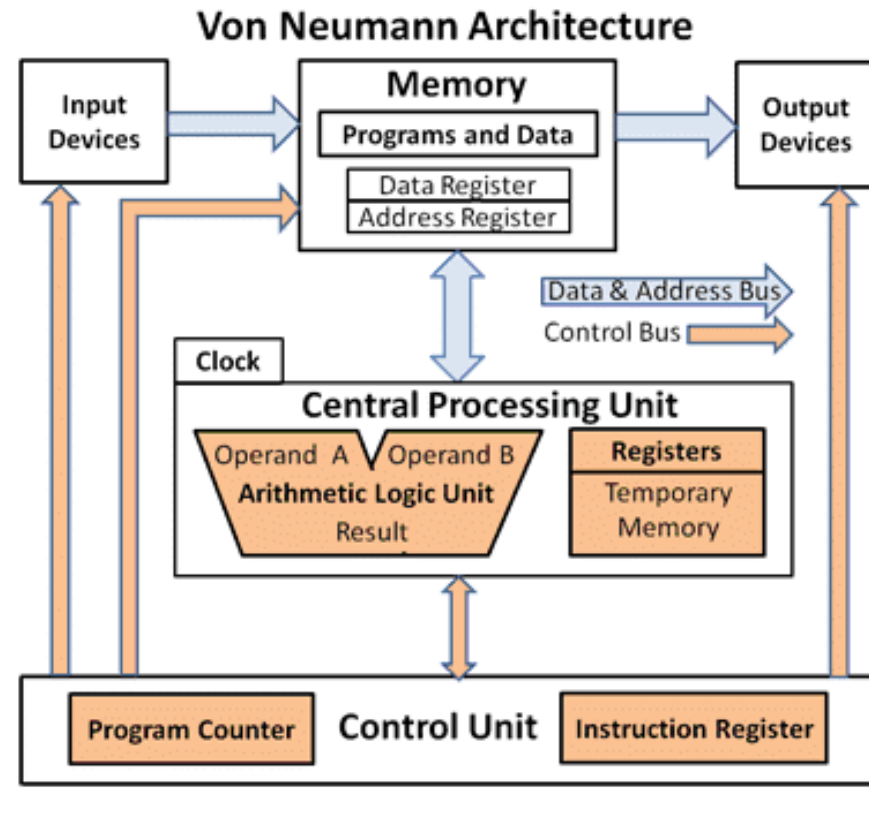


Illustration of the Harvard Architecture that uses two memories, one to hold programs and another to store data.

- ▶ Non- Von Newmann Representation
 - ▶ Non Von Newmann Computer Machines
 - ▶ Quantum Computers
 - ▶ Harvard Architectures
 - ▶ Hybrid Computers (or Post Moore Architectures)
- ▶ Processor
- ▶ Data Memory
- ▶ Instruction Memory
- ▶ Output

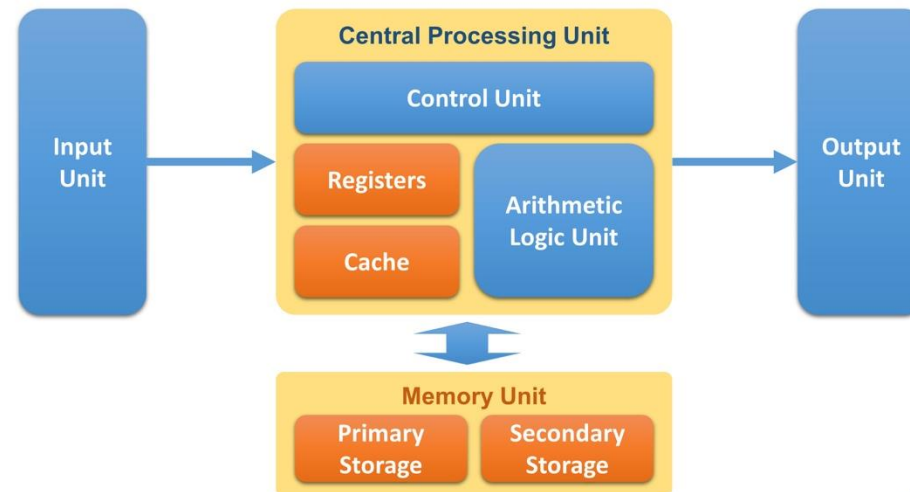
From <https://eca.cs.purdue.edu/index.html>

Von Neumann Architecture Representation in Detail

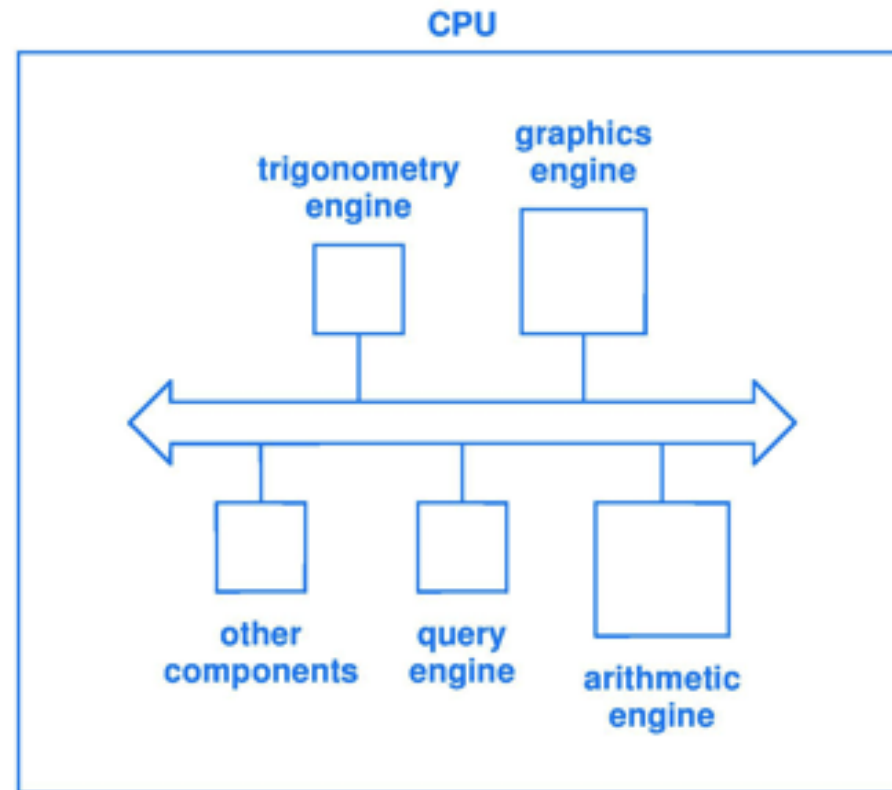


The CPU: Central Processing Unit

Computer Architecture



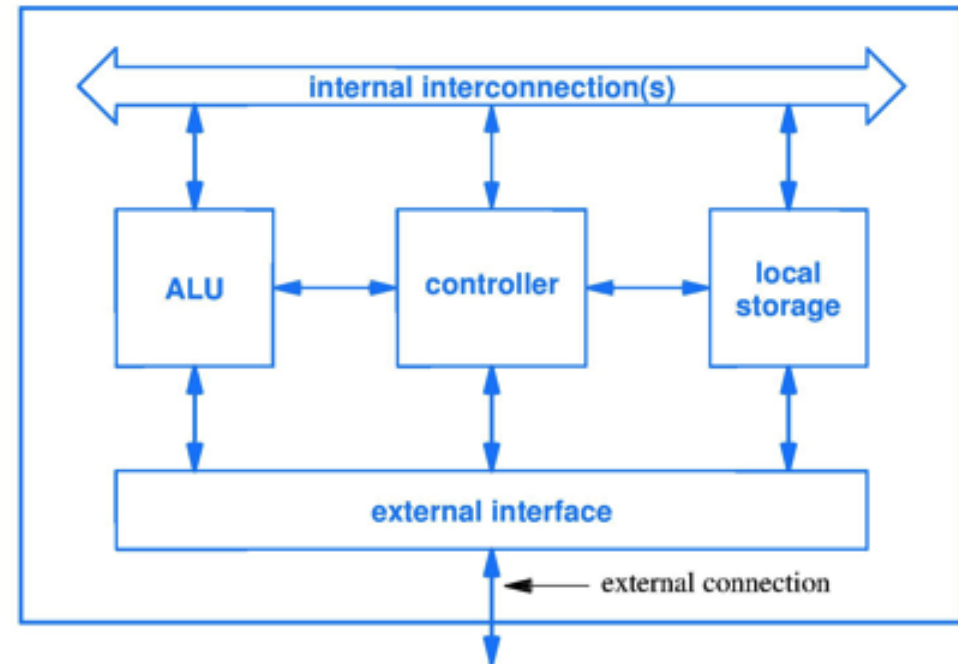
Processors Representation



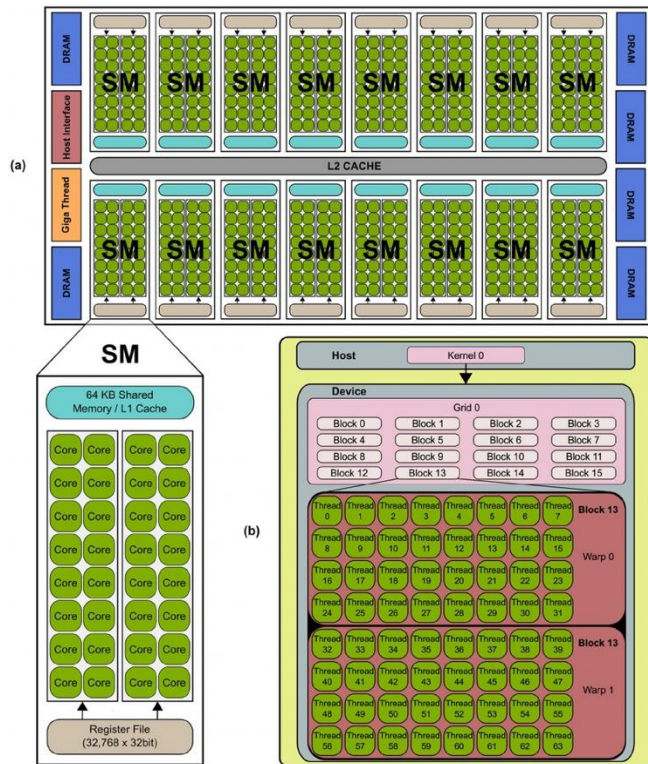
Processor Structure Representation

Conceptual Units:

- Controller
- Arithmetic Logic Unit (ALU)
- Local Data Storage (Registers)
- Internal Interconnections
- External Interfaces (I/Os)



More than CPUs: GPUs, FPGAs, TPUs, QPUs...

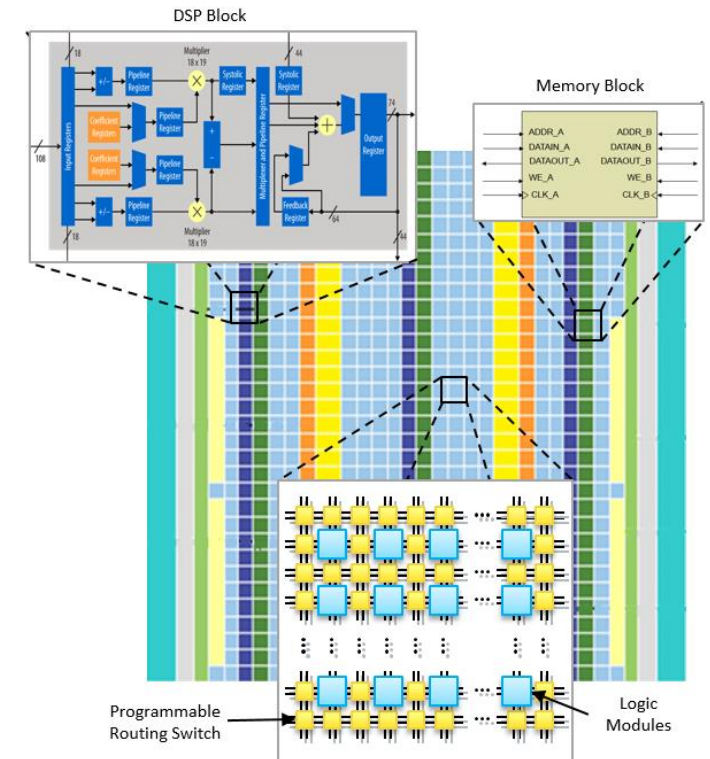


GPU



Source: NVIDIA

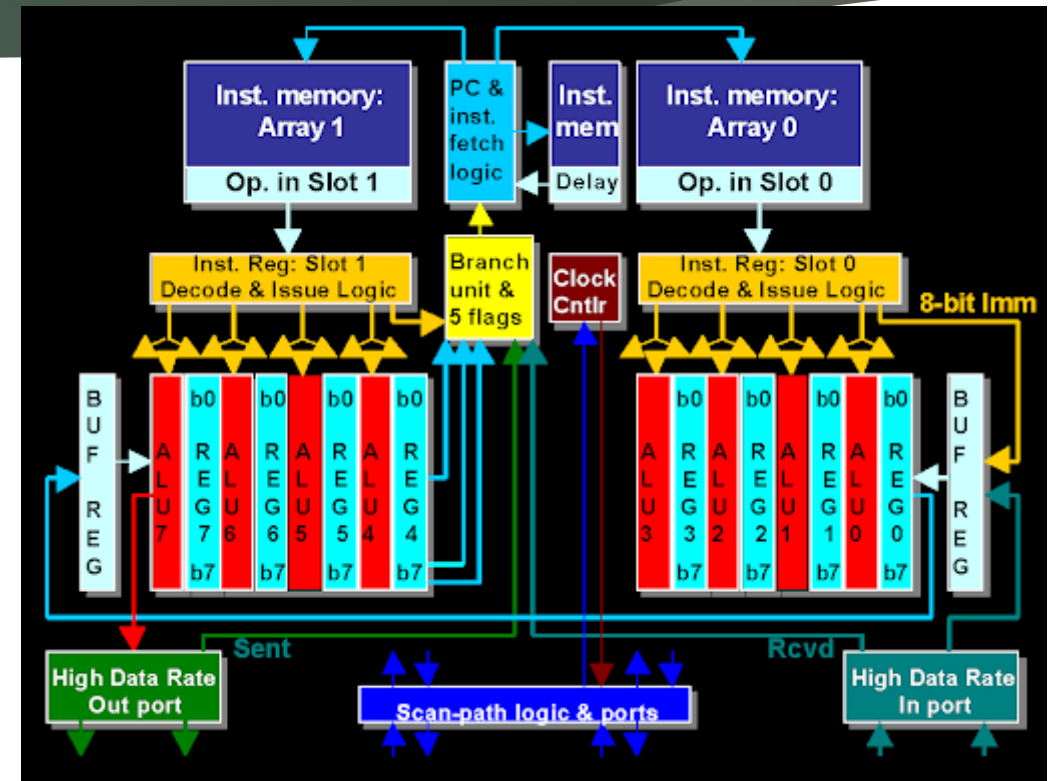
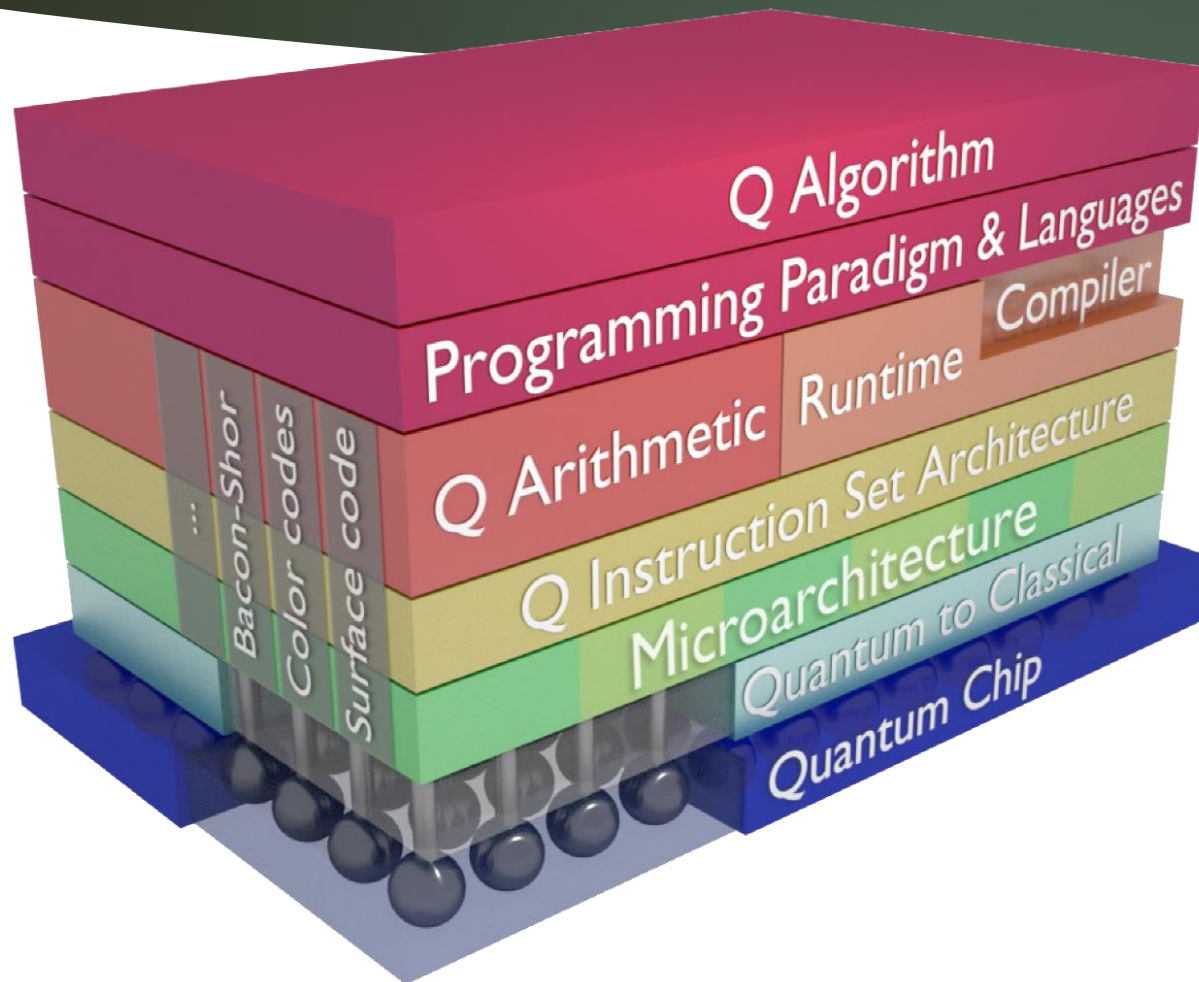
TPU



FPGA

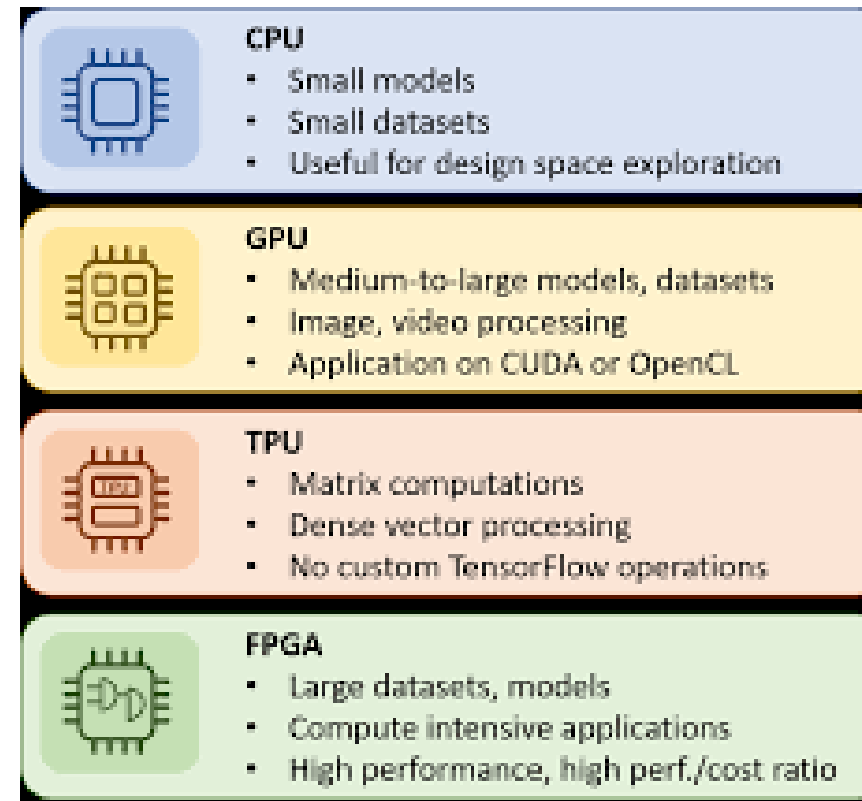
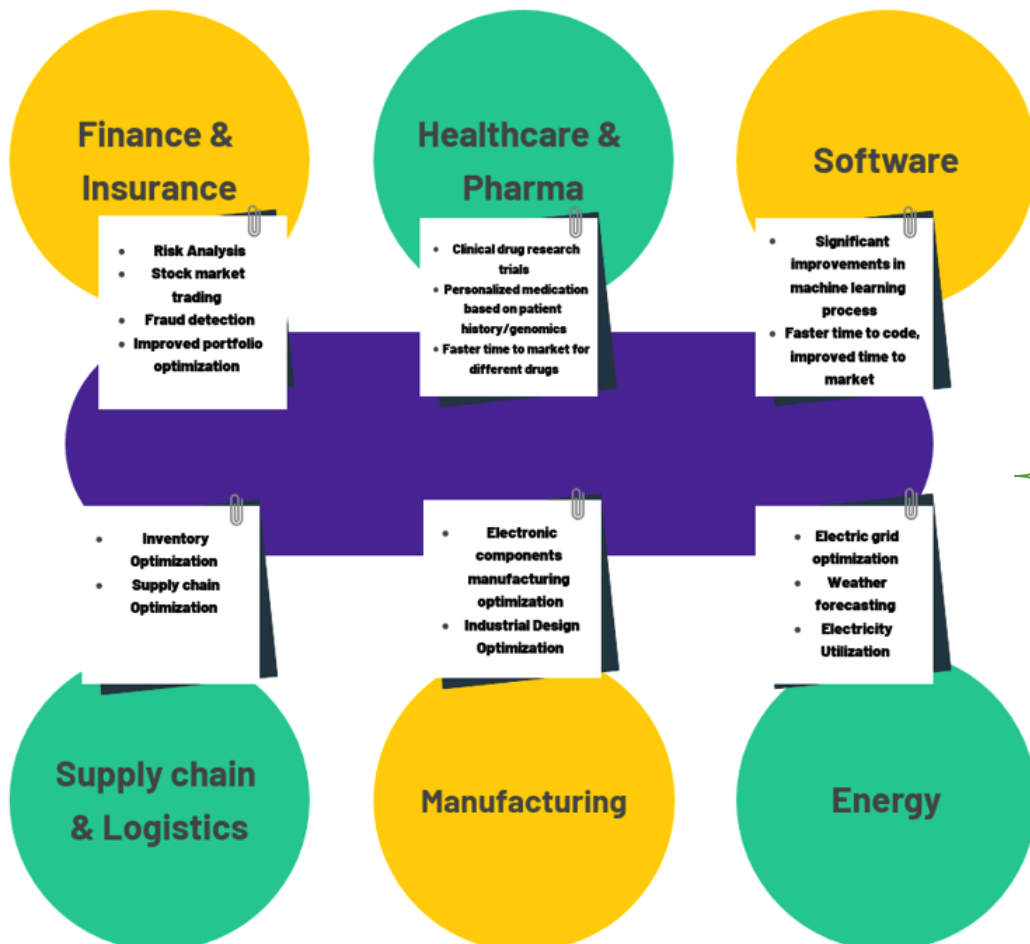
Quantum Processor Unit Architecture*

17



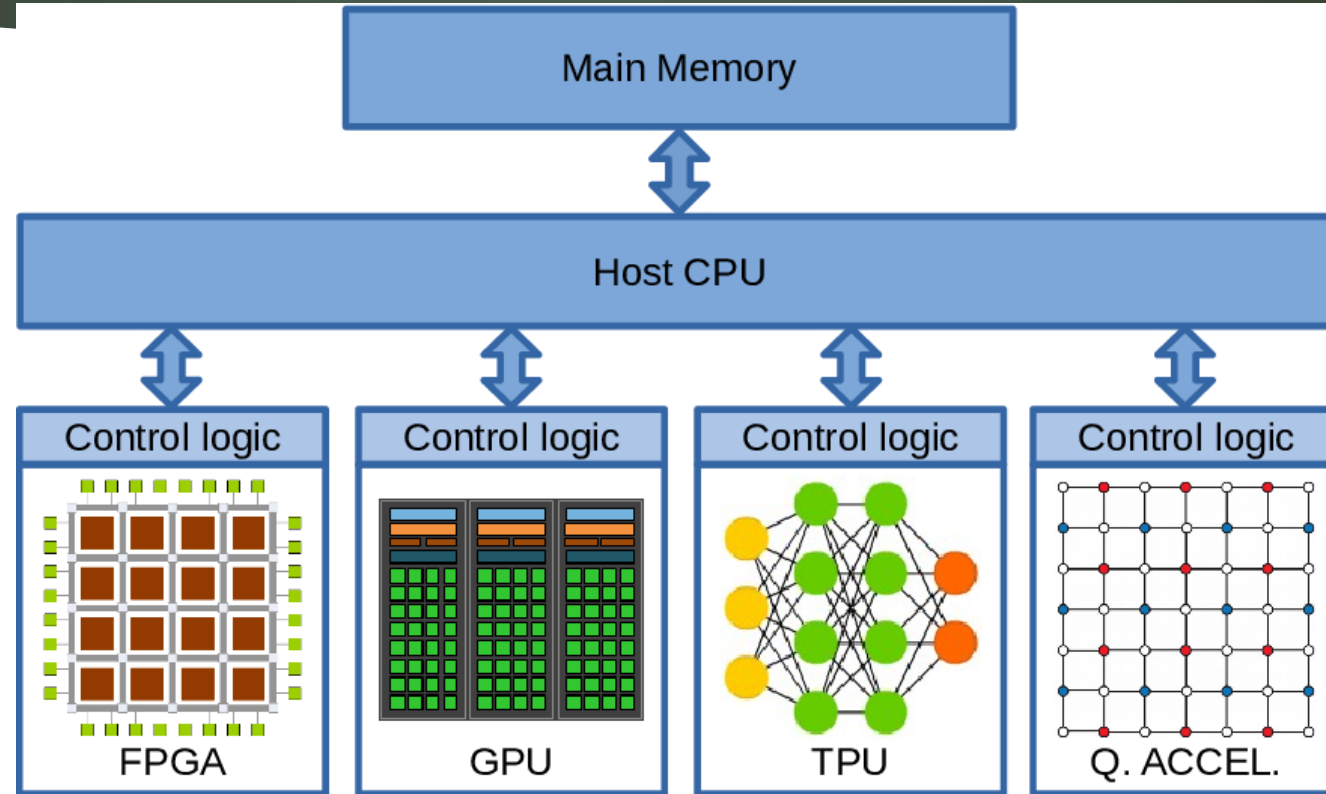
*Simplest Approach

Each PU for Specific Requirements



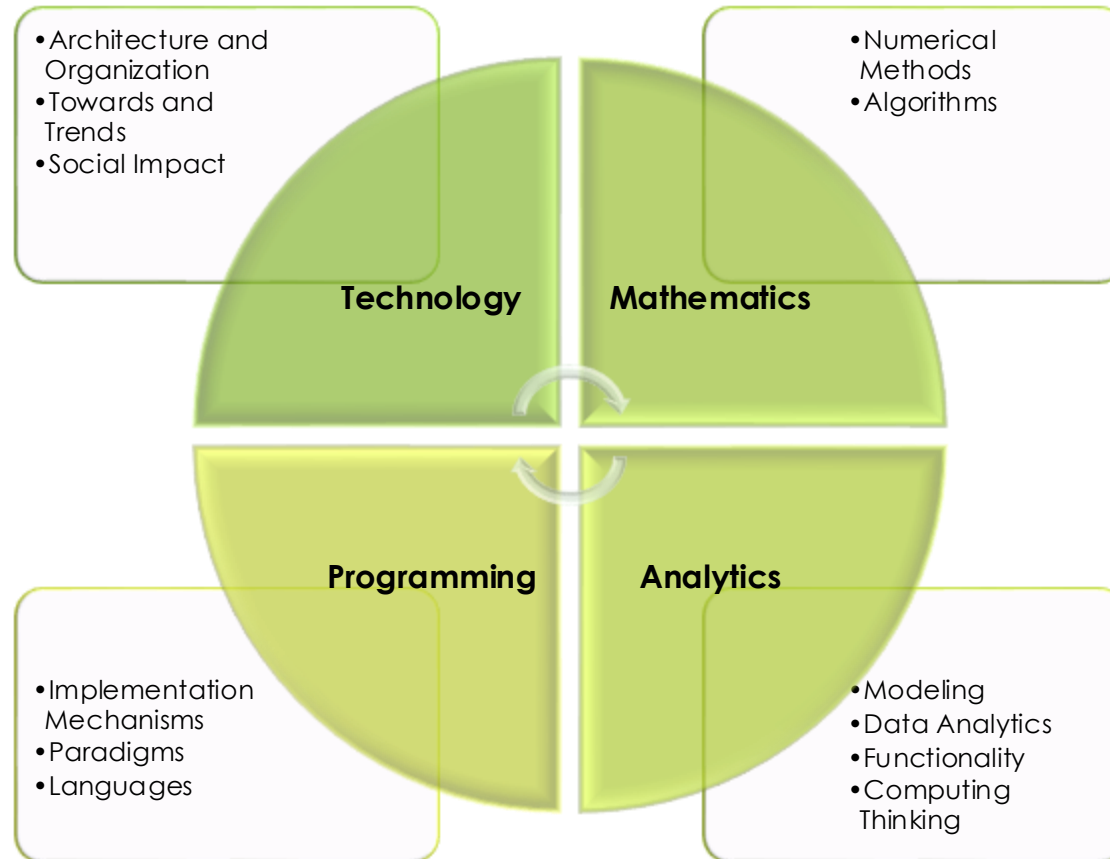
And QPUs

(New) Computer Architectures



From : Bertels, K., Sarkar, A., Hubregtsen, T., Serrao, M., Mouedenne, A.A., Yadav, A., Krol, A.M., Ashraf, I., & Almudever, C.G. (2020). Quantum Computer Architecture Toward Full-Stack Quantum Accelerators. IEEE Transactions on Quantum Engineering, 1, 1-17.

Computer Knowledge



Sustainability and Durable Computing Technology

Long-term viability involving low energy consumption and affordable costs of production, maintenance, and use.

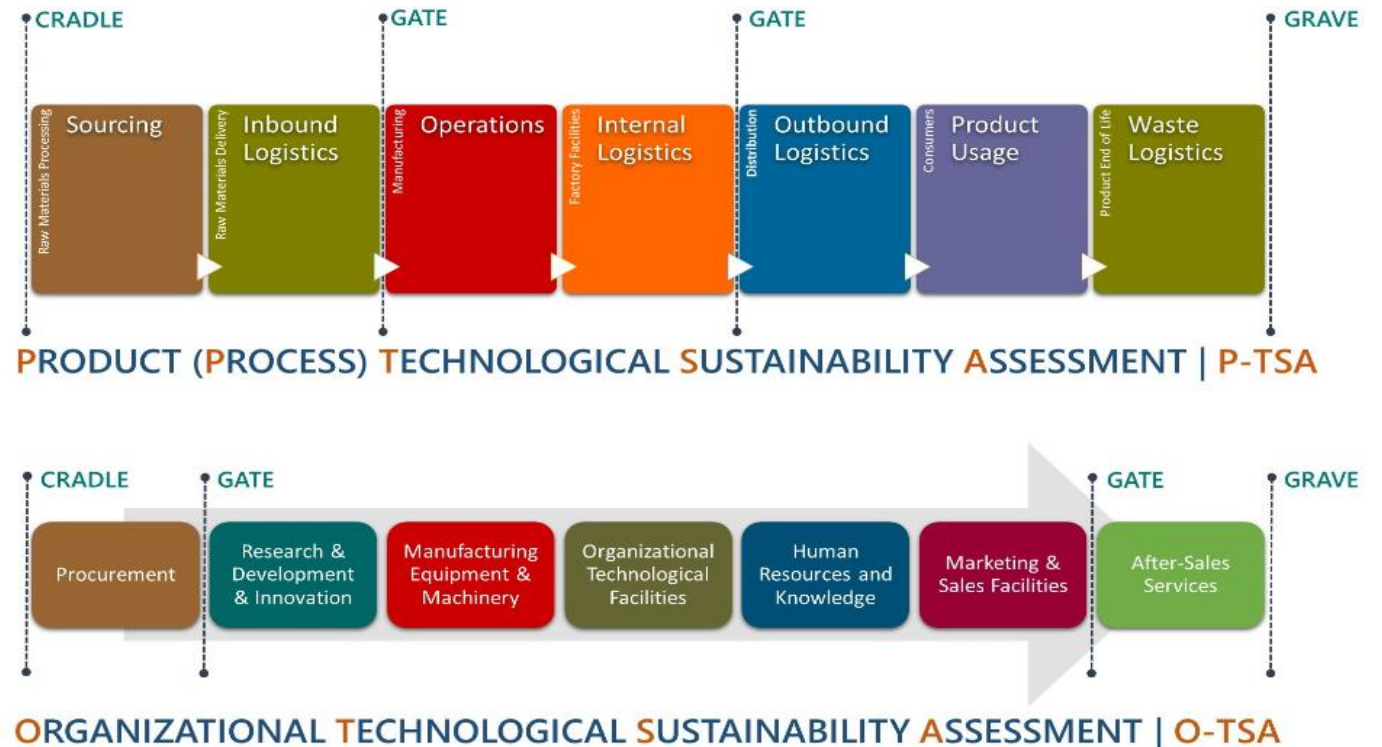
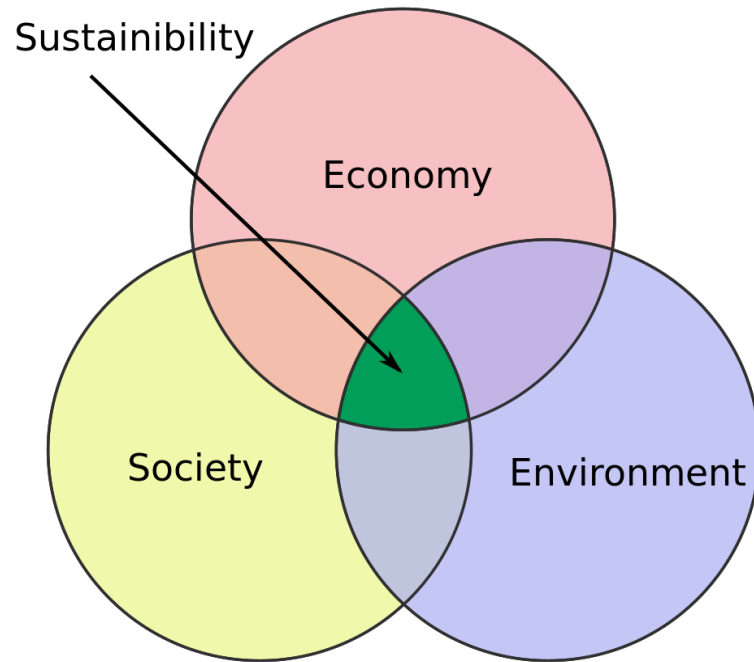
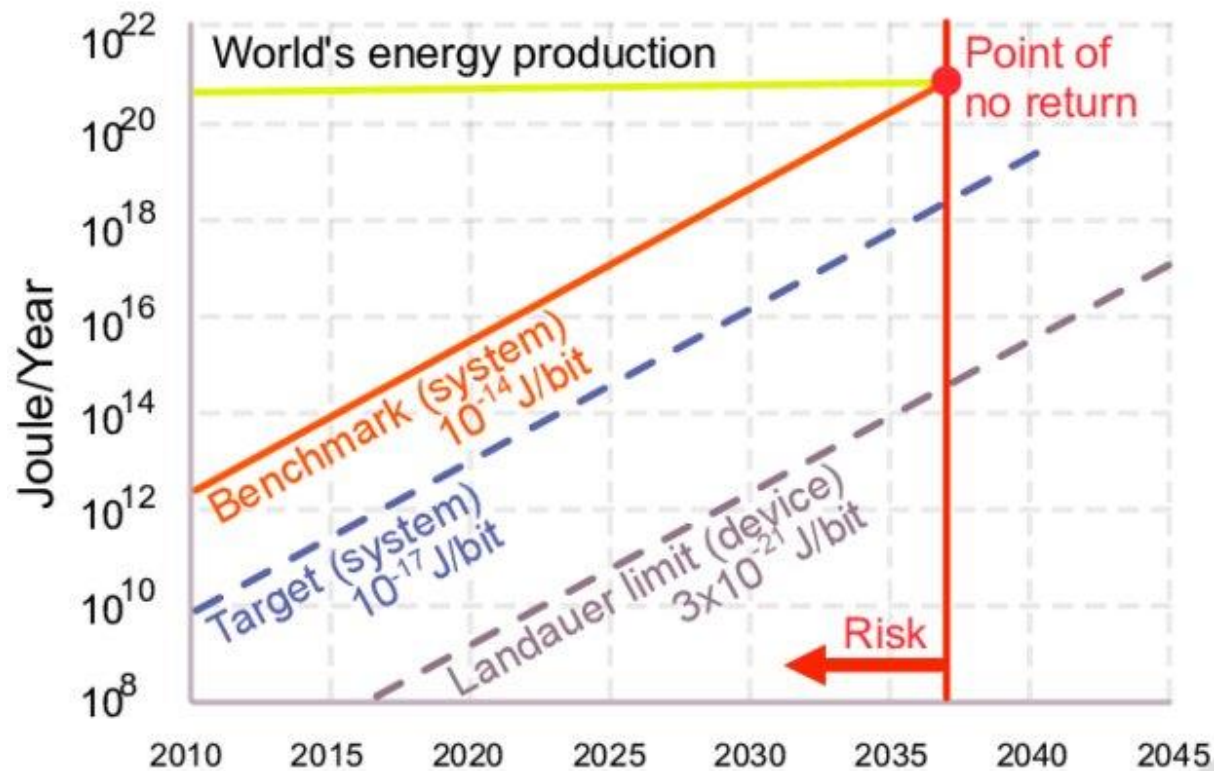


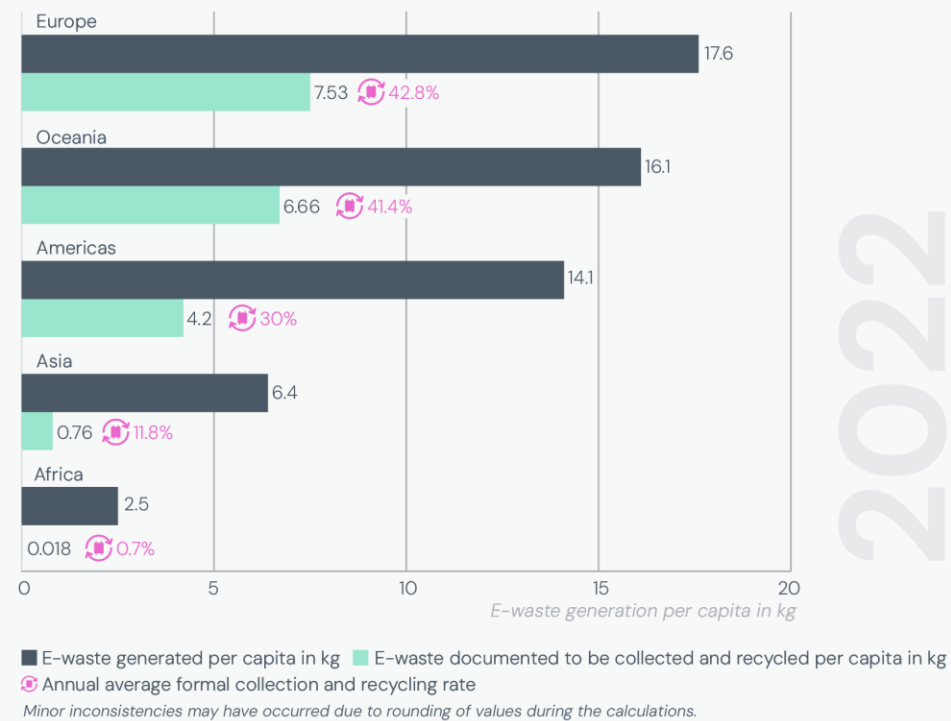
Figure 1. Life cycle approach to assessing product/process (P-TSA) and organizational (O-TSA) technological sustainability.

Vacchi, M.; Siligardi, C.; Demaria, F.; Cedillo-González, E. I.; González-Sánchez, R.; Settembre-Blundo, D. Technological Sustainability or Sustainable Technology? A Multidimensional Vision of Sustainability in Manufacturing. *Sustainability* **2021**, *13*, 9942. <https://doi.org/10.3390/su13179942>

Energy and E-Waste



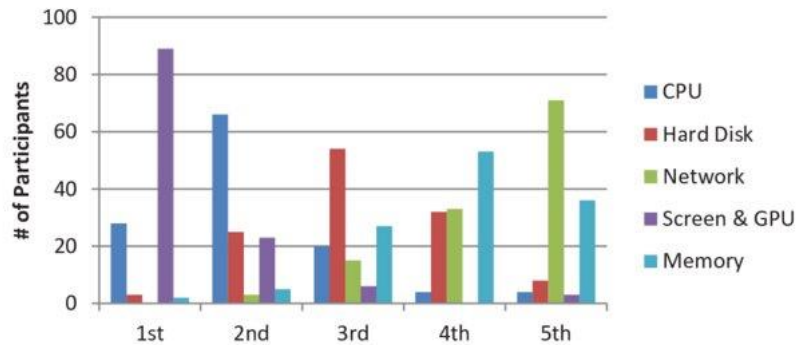
Amount of E-waste Generated and Collected



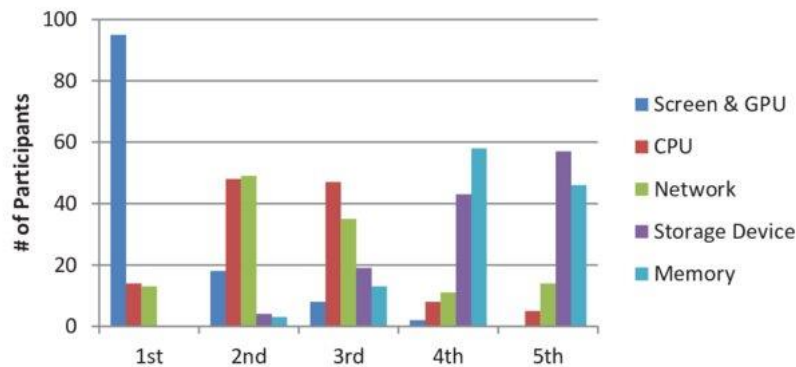
2022

Digital World and Energy Consumption Growth

(a) Desktop Computer Components Ranked by Energy Consumption



(b) Mobile Device Components Ranked by Energy Consumption



From Pang, Candy & Hindle, Abram & Adams, Bram & Hassan, Ahmed E.. (2015). What do programmers know about the energy consumption of software?. 10.7287/PEERJ.PREPRINTS.886.

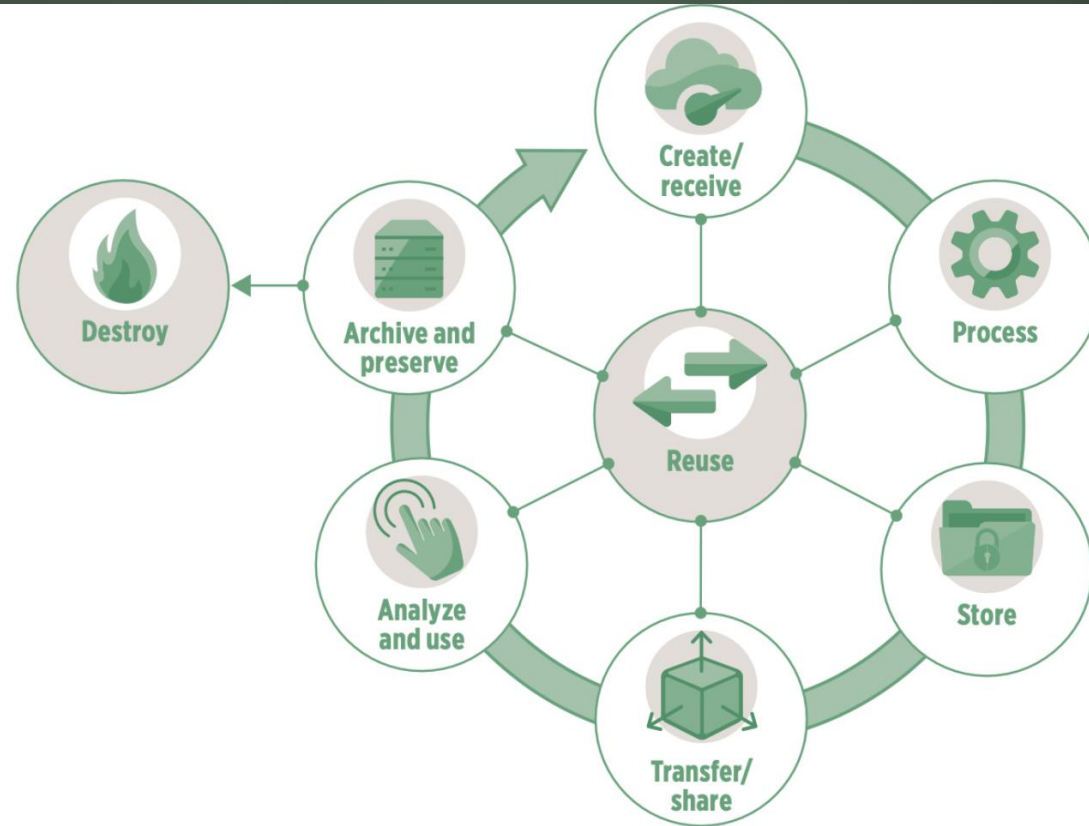
Evolution	2010	2015	2020	2025
Users (million)	2 023	3 185	4 700	5 500
Devices (million)	13 531	18 405	19 041	20 278
Equipment level	7	6	4	4
IoT (million)	1 000	9 605	20 315	48 272
Devices incl. IoT (million)	14 531	28 010	39 356	68 550
Mass (million tonnes)	128	164	236	317

The digital world from 2010 to 2025

F. Bordage. Study available in: https://www.greenit.fr/wp-content/uploads/2019/11/GREENIT_FENM_etude_EN_accessible.pdf

The number of devices sold (computer, gaming console, etc.) stabilises from 2015 (+ 10% only between 2015 and 2025), with the notable exception of the number of connected objects which is multiplied by 48 in 15 years (48 billion in 2025)

Data Cycle of Life



Source: WDR 2021 team.



About the Course

- Theoretical Magisterial Sessions
 - Conducted by C. J. Barrios Hernández, PhD.
- Theoretical - Practical Sessions
 - Conduced by SC3UIS and CAGE Team
 - Special Guest: Postgraduate Students
 - Special Seminars
 - Invited People of Research Centers or Industries
- Webminars and Video Talks
 - TED or others...

Goals

This is a course of Computer Architecture addressed to Systems Engineering, Informatics and Computer Science Students.

- Being able to locate oneself in the State of Art of Computer Architecture (from our point of view)
 - Handle terminology and technical specs.
 - **Promote Self-Learning.**
 - Understand the link between knowledge, technology and performance.
- **Understand (without fear) computer technology.**

About Teaching and Instruction



- **Carlos Jaime Barrios Hernández, PhD.** cbarrios@uis.edu.co [@carlosjaimebh](https://twitter.com/carlosjaimebh)
 - Director of High Performance and Scientific Computing Centre SC3UIS (www.sc3.uis.edu.co) and CAGE Research Group Director
 - Associate Professor EISI/UIS (<http://cormoran.uis.edu.co>)
 - Systems Engineering UIS, Bucaramanga, Colombia (2002), Master in Mat. Applied, Systems and Informatics UJF-Grenoble I, Grenoble, France (2005), Computer Science and Informatics Doctor, UNSA, Nice-Sophia Antipolis, France (2009), PostDoctoral Research, I3S/CNRS, Sophia Antipolis, Francia (2010).
 - Researcher in Advanced, High Performance and Scientific Computing (LIG, I3S/CNRS, INRIA (France), GPPD/UFRGS (Brazil), SC3UIS (Colombia)) and International Instructor in HPC and SC (ICTP/UNESCO (Italy), SCCAMP).
 - Chair of the Advanced Computing System for Latin America and Caribbean (SCALAC)
 - NVIDIA Deep Learning Institute Instructor
- **SC3 and CAGE Team** (More Information in www.sc3.uis.edu.co)

Contact: EISI Block: LP 226 and SC3 Space 4to Floor CENTIC

Please, Send an email for Rendez-vous



Course Highlights

- **58 Hours Program**
- **Theoretical – Practical Course**
- Theoretical Sessions (Starts at 0XX:10)
- Theoretical – Practical Sessions (Starts at XX:00)
 - **Please Punctuality!**
- About deliveries and evaluations
 - **Observe format, rules, time, and deadline (date and hour)**
 - **Please read the recommendations carefully**
- All course information is in:
http://wiki.sc3.uis.edu.co/index.php/Arquitectura_de_computadores
- AutoLearning !!



Content

1. Historic Development and Perspectives
2. Arithmetic of Computers
3. Computer Abstractions and Technology
4. Machine Programming and Linking
5. Processors and Memory
6. Storage and I/O
7. Multicores and Multiprocessing
8. Graphics and Visualization
9. Hot Topics and Trends

Evaluation

- All Updates are in the course site
[http://wiki.sc3.uis.edu.co/index.php/Arquitectura de computadores](http://wiki.sc3.uis.edu.co/index.php/Arquitectura_de_computadores)
- Individual Work-First Note
- Theoretical Practical Sessions (In groups)
- Project Class (In groups)
 - Advance Report
 - White Paper
 - Digital Poster
- Individual Formal Evaluation - Final
- BONUS (+0,3 max. in each evaluation: (Quiz, group performance, attendance, Questions in the Course)



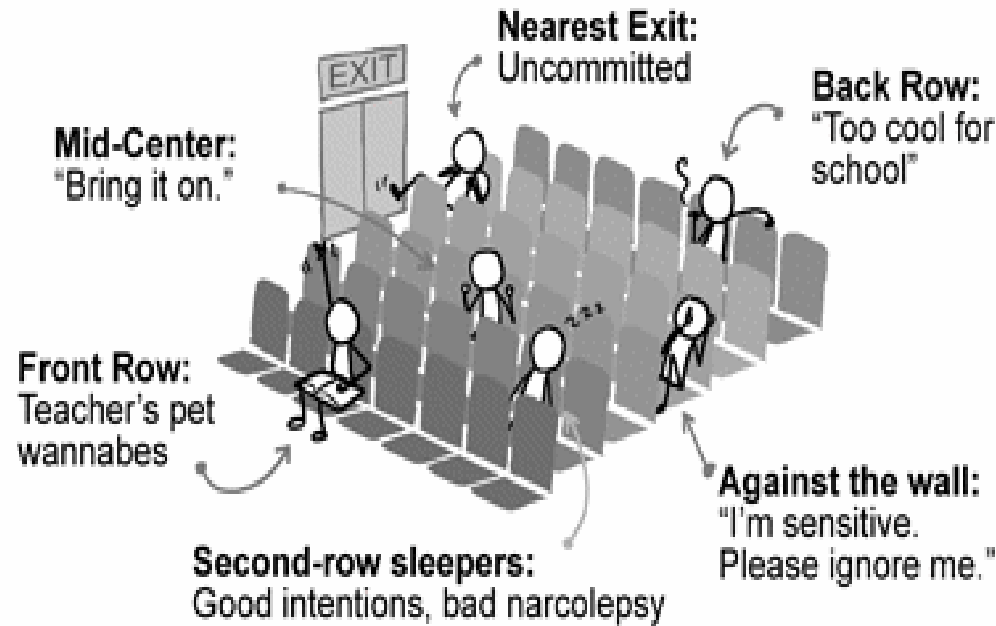
Important Notes

- All Available materials in English (International Technical/Scientific English)
- Bibliography and other resources are available in the site of the course. **This material is used for evaluations.**
- Attention to Students : (**Please, Send an email before for Rendez-vous**)
- **By default, the communication is via email from cormoran-web utility or email direct (cbarrios@uis.edu.co).**

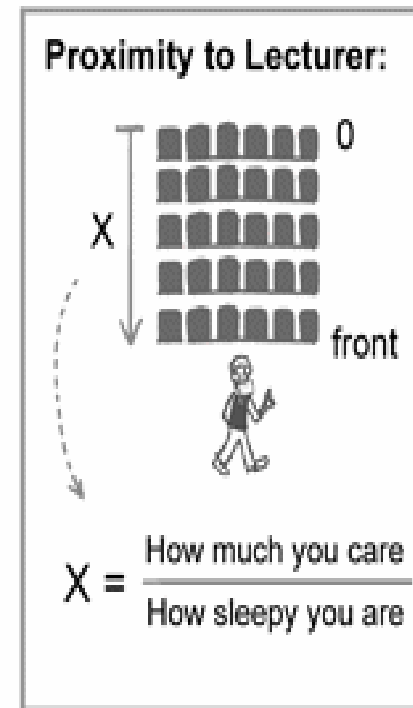
Questions?

WHERE YOU SIT IN CLASS/SEMINAR

And what it says about you:



WWW.PHDCOMICS.COM



JORGE CHAM © 2008